JULY 9–13, 2023

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SAN FRANCISCO, CA, USA

An Efficient and Cost-effective Method to Detect and Analyze ESD CDM Risks in Designs

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Problem Statement and Motivation

- **Checking ESD CDM Risk**
  - The device is initially charged (during handling) and then discharges through a grounded pin.
  - Discharge current results in voltage build-up across Gate-Source of MOS which may cause breakdown.
  - Ideally, CDM risk needs to be determined by transient simulation with the following requirements
    - Electrical modelling of substrate, devices, metal network and package for CDM event
    - Modelling of CDM current injection in the substrate and then discharge happening at every pad individually
    - Measurement of voltage build-up across Gate-Source of every MOS and comparison w.r.t. breakdown voltage
- **Complexities of Simulation Based CDM Checking**
  - Modelling : Distributed modelling of the substrate, devices, metal network and package together for CDM event is very complex
  - Resource requirements
    - Even if a distributed model is available, simulating that is a massive runtime and capacity challenge
    - There is no complete ready-made solution available in the industry which can handle all designs

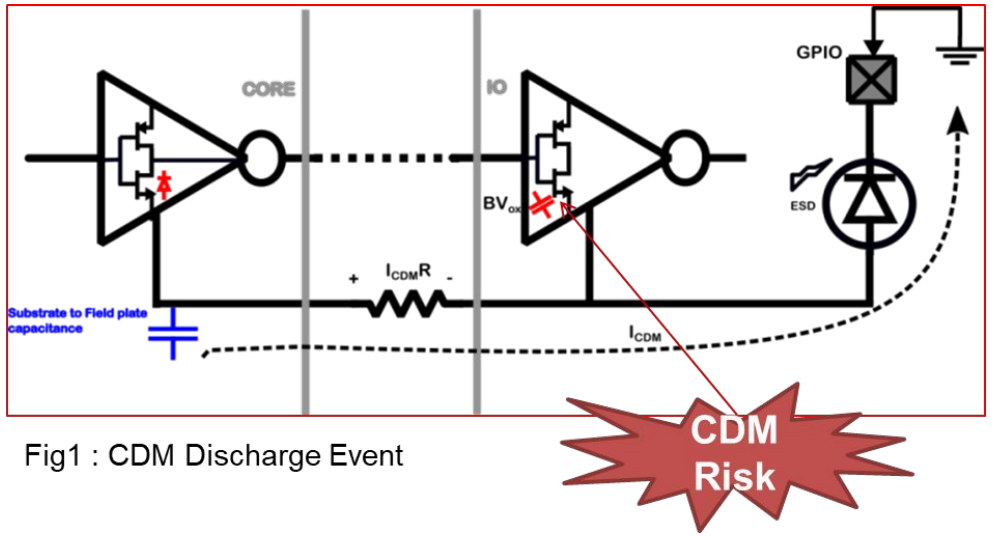

Fig1 : CDM Discharge Event

Proposed Solution

- **Requirements of the solution**
  - Setup : Schematic level analysis with netlist
  - Efficient : Ability to handle multi-million transistor designs
  - Cost Effective : No simulation. Only relying on topological detection and analysis
  - Actionability : Focus on the true risks which need additional corrective action
- **Overview of the solution : Multi-stage Coherent Risk Identification and Analysis**
  - **Detection**
    - Prework : Map the CDM Risk to efficient, simple Generic CDM Critical Signatures/Patterns
    - **Stage 1** : Detect Generic CDM Critical Topology Instances using the Pattern Matching
  - **Analysis** of identified risks in context of the design scenarios and protection mechanisms applicable for CDM
    - **Stage 2** : Analysis of protection by Extrinsic Circuits (Primary and Secondary ESD clamps) and filtering out protected instances
    - **Stage 3** : Analysis of CDM risk relevance of domains and filtering out the detected instances from irrelevant domains

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Detect Generic CDM Critical Topology Instances (Stage 1)

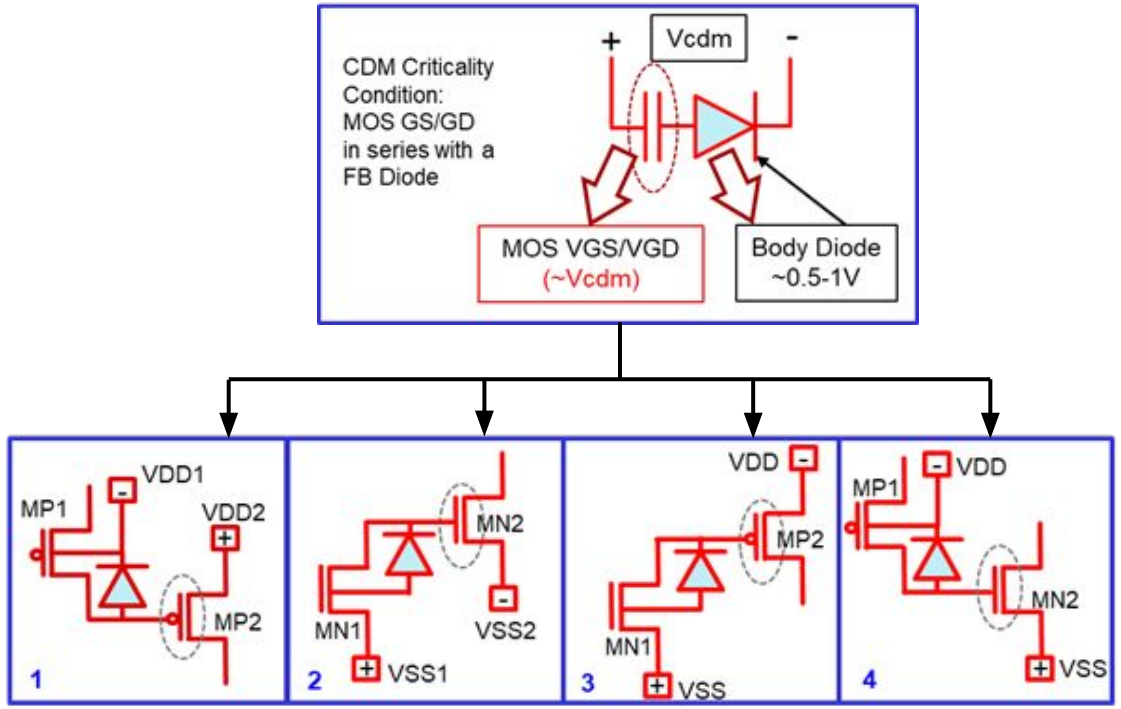
Risk analysis with complete CDM-relevant information

Stages 2,3,4 : Progressive Filtering with #Instances to be analyzed reducing with stages

Report Actual Risks after 3 stages Filtering

1. Detection of Generic CDM Critical Topologies

- **CDM Critical Topology Signature Definition**
  - A MOS gate-source between two different power or ground pads(domains) with one forward-biased parasitic diode (Body diode) in series : **Maximum CDM Stress across Gate-Source □ Maximum Risk of Gate Oxide Breakdown**

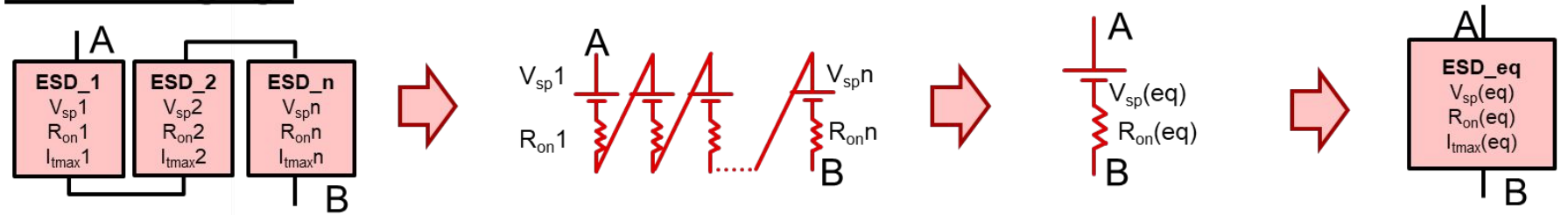


- **CDM Critical Topology manifestation**
  - Driver PMOS(VDD1) – Receiver PMOS (VDD2) □ Cross Domain
  - Driver NMOS(VSS1) – Receiver NMOS (VSS2) □ Cross Domain
  - Driver NMOS(VSS) – Receiver PMOS (VDD) □ In/Cross Domain
  - Driver PMOS(VDD) – Receiver NMOS (VSS) □ In/Cross Domain
- **Limitation of Generic CDM Critical Topology Detection**
  - Generic in nature : A CDM critical topology may not lead to an actual CDM Risk, but **a potential risk**.
  - Need to analyze with **Impact of Protections** (Stages 2 and 4) and **Electrical Relevance of Domains** (Stage 3) around the detected CDM Critical Topology in order to qualify the risk

2. Analysis of Extrinsic ESD Protections

- Primary ESD protection devices for CDM
  - The robustness of the primary ESD network for discharging the peak CDM current is checked in this algorithm (voltage build-up in the ESD network (Vcdm) checked against VBD of the MOS)
  - **Proposed algorithm does this without any simulation**
    - Utilizes a direction aware Thevenin reduction algorithm to solve the ESD network handling all elements in series and/or parallel connection to determine Vcdm (Vsp + Icdm * Ron) and Itmax

Series Merging :

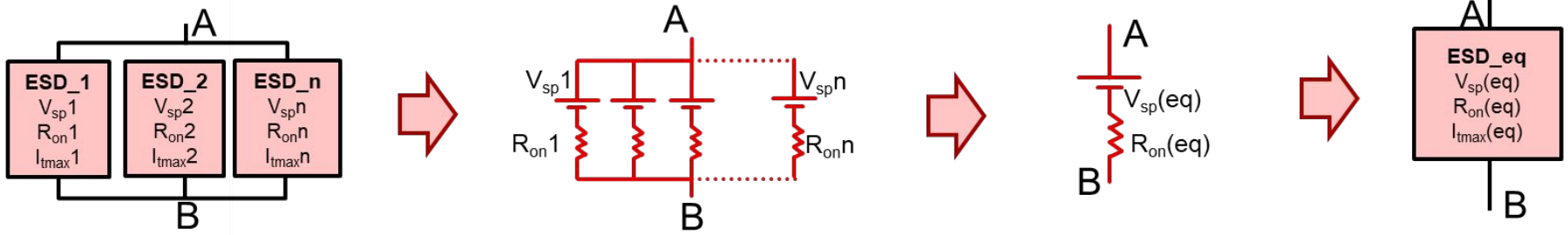


$V_{sp}(eq) = \sum_{i=1}^{n} Vspi$

$R_{on}(eq) = \sum_{i=1}^{n} Ri$

$I_{tmax}(eq) = \min(It1, It2..)$

Parallel Merging :



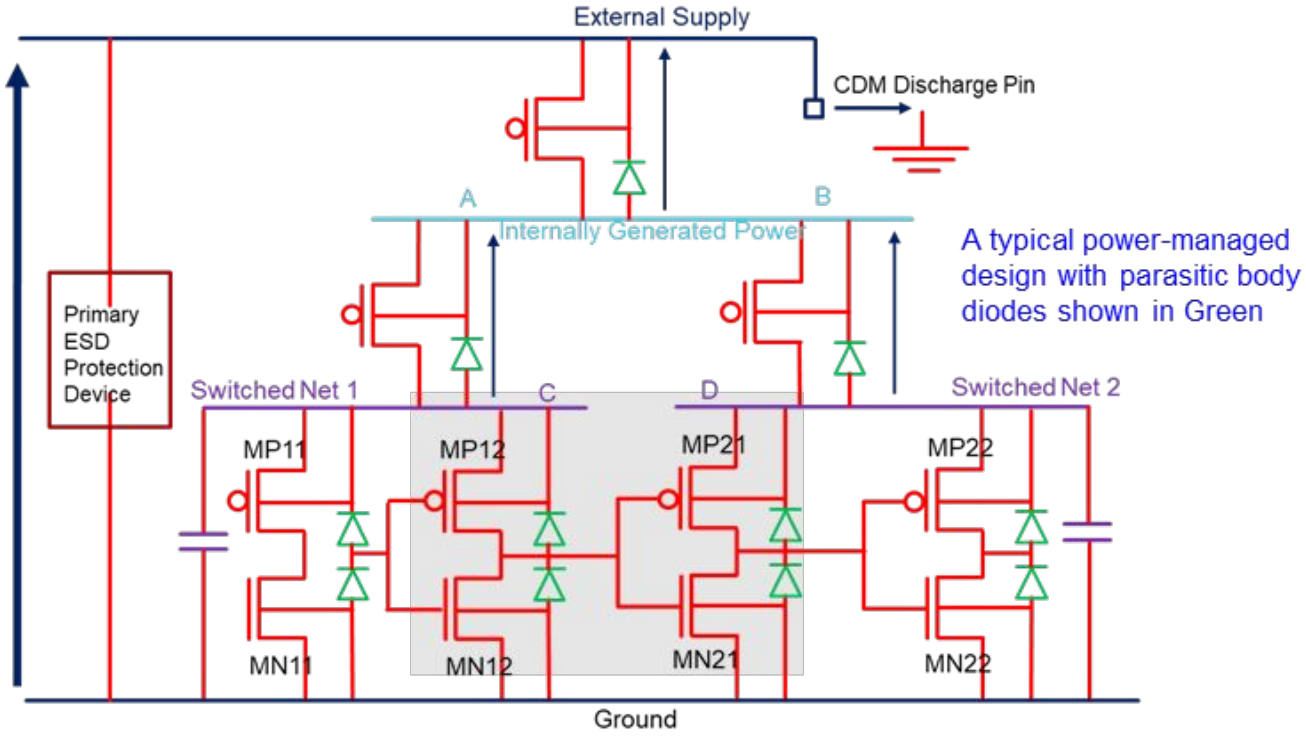
$$V_{sp}(eq) = \frac{\sum_{i=1}^{n}\left(\frac{Vi}{Ri}\right)}{\sum_{i=1}^{n}\left(\frac{1}{Ri}\right)}$$

$$R_{on}(eq) = \frac{1}{\sum_{i=1}^{n}\left(\frac{1}{Ri}\right)}$$

$I_{tmax}(eq) = \sum_{i=1}^{n} Iti$

3. Analysis of Domain's Relevance on CDM Risk

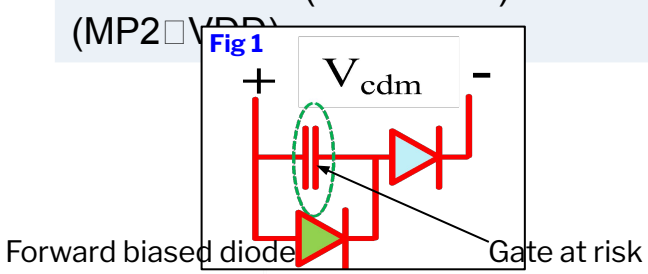
- The CDM risk is dependent on the Power-domains (whether External or Internal/Switched) and some electrical parameters of Driver and Receiver Domains
- The CDM risk for a driver-domain and receiver-domain combination can be ignored if certain electrical parameters of Driver and Receiver Domain satisfy certain threshold values : **CDM Risk Free Domains**
- Previously detected Generic CDM critical topologies from this kind of CDM Risk Free will not need any further action.
- E.g. For the circuit shown in Fig :
  - Electrical Parameters for Switched Net 1 and Switched Net 2 needs to be analyzed
  - If the domains are CDM irrelevant, the CDM risky topologies (shown by grey box), would be filtered out

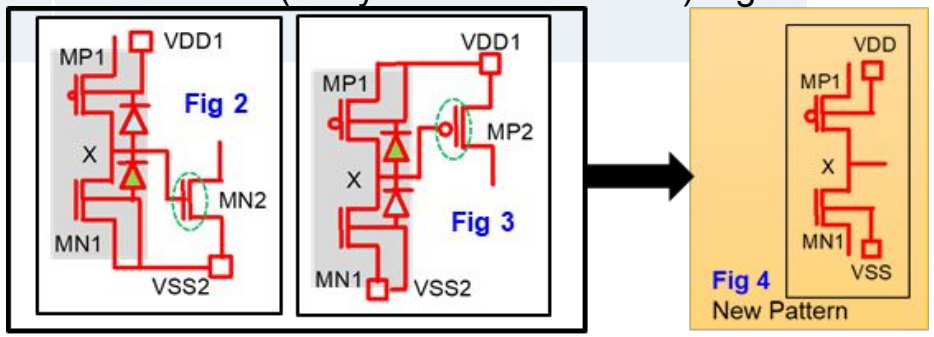


4. Analysis of Intrinsic Clamps/Protections

- A CDM Risk Topology may have other functional circuitries around, which can act as a clamp (Forward bias diodes) across the Gate at risk, limiting G-S voltage build-up (Fig 1)

CDM Critical Topology	Intrinsic Clamp
Driver PMOS (MP1□VDD) – Receiver NMOS (MN2□VSS)	NMOS MN1 (Body Diode VSS□Gate) Fig 2
Driver NMOS (MN1□VSS) – Receiver PMOS (MP2□VDD)	PMOS MP1 (Body Diode Gate□VDD) Fig 3

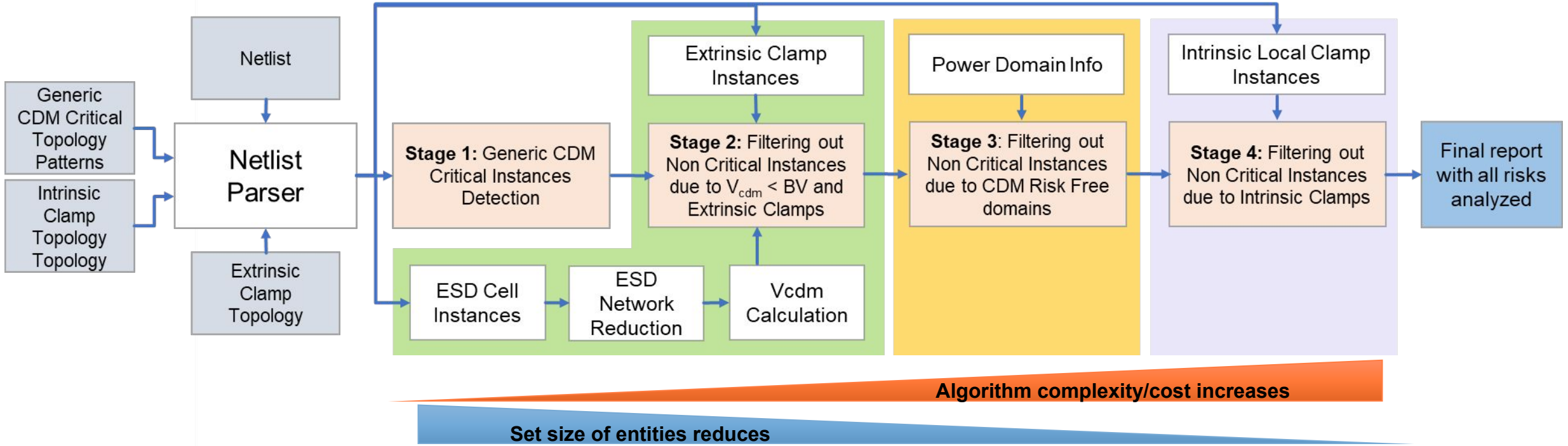




- **Proposed solution detects intrinsic protection efficiently**
- **New identification algorithm introduced** for **"Protected Net (X)" detection** (only one 2-MOS pattern (Fig 4)) instead of conventional "Protected Receiver MOS" detection (Two 3-MOS topologies (Fig 2 and 3))
- Runtime is drastically improved, **>15x w.r.t. conventional 3-MOS topology search**

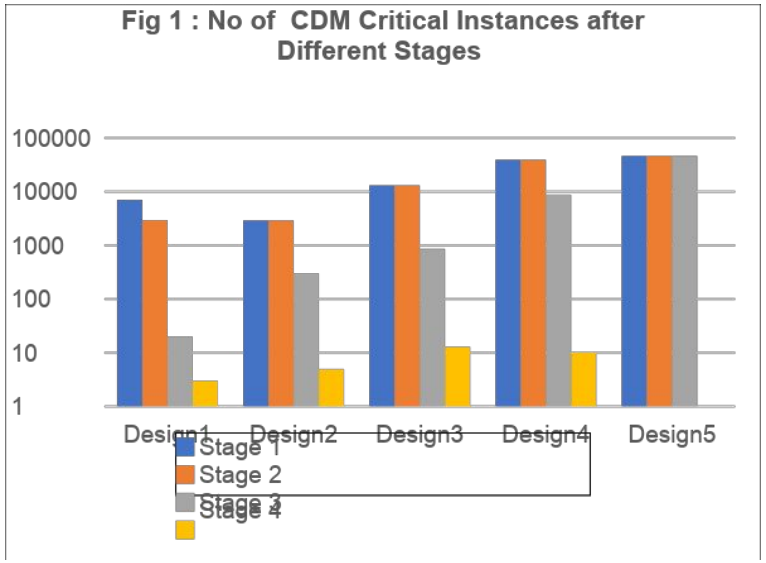
Final Solution Flow Chart

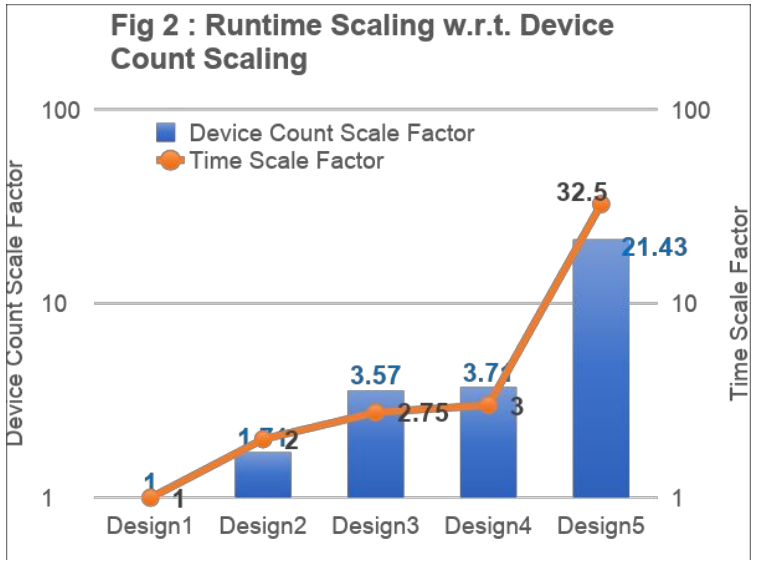
- The final solution view integrating the different stages of decision making together
- A coherent detection and multi-stage progressive risk analysis mechanism is implemented
  - Includes a simple, less error-prone detection mechanism
  - Ensures the most complex (costly) steps are applied on an reduced set of entities
  - Makes the solution efficient and cost-effective



Results and Summary

- Results
  - The **coherent CDM Risk Identification and Analysis solution helps in reducing false violations and draws attention to real risk**.
  - Most designs benefit from the multi-stage risk assessment, while one Design5 had all risks mitigated at Stage 4 (Fig 1)
  - Runtime is fairly scalable and can handle multi-million MOS netlists without any issue (Fig 2)





- The solution efficiently detects and analyzes CDM risk in designs, without running a complex simulation
  - **Accurate & Robust** : No false detection. Simple detection followed by progressive filtering based on context. Only Real threats are highlighted eventually.
  - **Capacity to handle any design netlist** : Progressive filtering ensures complex, costly identifications are done later when the entity-set is reduced

Questions?